IN THE CLAIMS:

1. (Original) A structure having an abrupt doping profile comprising:

a single crystal semiconductor substrate having an upper surface,

a first epitaxial layer of Ge over said upper surface,

said first epitaxial layer having a thickness less than the critical thickness,

said first epitaxial layer having a concentration of dopant greater than 5×10^{19} atoms/cc, said dopant selected from the group consisting of phosphorus and arsenic, and

a second epitaxial layer of a semiconductor material over said first epitaxial layer.

Claim 2 (Original) The structure of claim 1 wherein said second layer comprises a material selected from the group consisting of Si and SiGe.

Claim 3 (Original) The structure of claim 1 wherein said first layer has a thickness in the range from 0.5 to 2 nm.

Claim 4 (Original) The structure of claim 1 wherein said second layer has a concentration change from said first layer into 40Å of said second layer of greater than 1×10^{19} atoms/cc.

Claim 5 (Original) The structure of claim 1 further including a third epitaxial layer of semiconductor material having a doping profile with a dopant concentration less than 5×10^{18} atoms/cc.

Claim 6 (Original) The structure of claim 1 wherein said second epitaxial layer having a thickness of at least 300 Å and having a doping of P less than 5×10^{16} atoms/cc for a predetermined thickness after its initial 300 Å thickness.

Claims 7-17 (Cancelled)

Claim 18 (Original) A method for forming abrupt doping within a semiconductor layered structure comprising the steps of:

selectively amorphizing a first layer having a high Ge content greater than 0.5, and

crystallizing said amorphized first layer by solid phase regrowth.

Claim 19 (Original) The method of claim 18 wherein said step of selectively amorphizing includes the step of ion implantation.

Claim 20 (Original) The method of claim 18 wherein said step of selectively amorphizing includes first forming second and third layers about said first layer, said second and third layers having a Ge content less than 0.5.

Claim 21 (Original) The method of claim 18 wherein said step selectively amorphizing includes the step of first forming said first layer having a Ge content greater than 0.5.

Claim 22 (Original) A field effect transistor comprising:

a single crystal substrate having a source region and a drain region with a channel therebetween and a gate electrode above said channel to control charge is said channel and

a first layer of Ge less than the critical thickness doped with a dopant selected from the group consisting of phosphorus and arsenic positioned below said channel and extending through said source and drain regions.

Claim 23 (Original) The field effect transistor of claim 22 wherein said layer of Ge is in the range from .5 to 2 nm thick.

Claim 24 (Original) The field effect transistor of claim 22 wherein said channel is in a second epitaxial layer selected from the group consisting of Si and SiGe formed over said first layer.

Claim 25 (Original) A field effect transistor comprising:

a single crystal substrate,

a first layer of Ge less than the critical thickness doped with a dopant selected from the group consisting of phosphorus and arsenic formed on said substrate,

a second layer of undoped SiGe epitaxially formed on said first layer,

a third layer of strained undoped semiconductor material selected from the group consisting of Si and SiGe,

a source region and a drain region with a channel therebetween, and

a gate electrode above said channel to control charge in said channel.

Claim 26 (Original) The field effect transistor of claim 25 wherein said layer of Ge is in the range of 0.5 to 2 nm thick.

Claim 27 (Original) A field effect transistor comprising

a single crystal substrate,

an oxide layer formed on said substrate having an opening,

a gate dielectric and gate electrode formed in said opening over said substrate,

a source and drain region formed in said substrate aligned with respect to said gate electrode,

a dielectric sidewall spacer formed on either side of said gate electrode and above a portion of said source and drain regions,

a first layer of Ge less than the critical thickness doped with a dopant selected from the group consisting of phosphorus and arsenic selectively positioned over exposed portions of said source and drain regions,

a second layer of semiconductor material selected from the group consisting of Si and SiGe doped with a dopant selected from the group consisting of

phosphorus and arsenic epitaxially formed over said first layer to form raised source and drain regions,

Claim 28 (Original) The field effect transistor of claim 27 wherein said layer of Ge is in the range from 0.5 to 2 nm thick.